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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/739,388
Filing Date: December 19, 2000
Appellant(s): YOUNG, GENE F.

Robert A. Greenberg
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 19, 2006 appealing from the Office action mailed June 15, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

The statement of the status of claims contained in the brief is correct.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,148,349	Chow et al.	11-2000
6,542,961	Matsunami et al.	04-2003
6,456,626	Whiting et al.	09-2002
5,739,777	Kaneko	04-1998
6,325,636	Hipp et al.	12-2001
6,199,137	Aguilar et al.	03-2001
5,465,357	Bealkowski et al.	11-1995

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 9-15, 18-22 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. (US 6,148,349) in view of Matsunami et al. (US 6,542,961).

Regarding claims 1, 9-11, 15, 18-20 and 31, Chow discloses a system module (fig. 2, items 226 and 802) to couple a switch fabric network (item 106) to shared I/O resources (items 224). The module comprises a first serverlet (figs. 2 and 3, item 212) and a second serverlet (figs. 2 and 3, item 214). The system module also comprises a second switching device (fig. 8, item 802; col. 25, lines 44-50) to couple to the switch fabric network and the first and second serverlets.

However, Chow does not disclose the first switching device and bus for coupling the serverlets to the I/O resources. Matsunami discloses stations (fig. 1, item 30) coupled to I/O resources (item 10; fig. 2) by a switch (item 20; fig. 3) and a data bus (items 21). The switch has a controller device (item 70), a switching device to couple the first interface device to the second interface device (fig. 1, item 20; note: port connections from each host to the switch), and has a third interface device (fig. 1, item 204). The switch comprises a many-to-one switching device (fig. 3, item 201) to couple the serverlets to a single bus interface (item 2020; fig. 18; col. 16, lines 12-13; note: multiple hosts can access one LU - fig. 15). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a first switching device and bus to couple serverlets to I/O resources in the invention of Chow in order to enhance scalability or improve reliability (Matsunami, col. 12, lines 4-14 and 25-40).

Regarding claims 2, 12 and 21, in Chow the I/O resources comprise a first disk system (fig. 2, item 218) and a second disk system (item 222).

Regarding claims 3-4 and 13, in Chow the serverlets each comprise memory devices and a processing unit (fig. 3, item 304), a first power conversion unit (item 306), and an inherent interface to couple the processing unit and the memory devices.

Regarding claims 5, 14 and 22, Chow discloses that the network (fig. 1, item 106) is Fibre Channel (col. 38, lines 7-13).

Regarding claim 6, in Chow a data bus (fig. 3, item 228) couples the second switching device to the serverlets.

Claims 7, 16 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. in view of Matsunami et al. as applied to claims 1, 11 or 20 above, and further in view of Whiting et al. (US 6,456,626).

Regarding claims 7, 16 and 23, Chow in view of Matsunami discloses a data bus (Chow, fig. 3, item 228) to couple the serverlets to the second switching device (Chow, fig. 8, item 802). However, Chow in view of Matsunami does not disclose a third switching device coupled to the switch fabric. Whiting discloses a backup network interface (fig. 5, item 150; col. 4, lines 28-32) connected to a switch fabric (item 10). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a third switching device coupled to the switch fabric in the invention of Chow in view of Matsunami in order to provide a redundant connection to the switch fabric in the event the primary switch or interface fails (Whiting, col. 4, lines 28-32).

Claims 8, 17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow in view of Matsunami and Whiting as applied to claim 7, 16 or 23 above, and further in view of Kaneko (US 5,739,777).

Regarding claims 8, 17 and 24, Chow in view of Matsunami and Whiting discloses a second switching device (fig. 8, item 802) coupled to a network (item 106). However, Chow in view of Matsunami and Whiting does not disclose a switching device comprising a first conversion unit, a second conversion unit and a switching device to couple the switch fabric to the first and second conversion unit. Kaneko discloses a first conversion unit (fig. 1, item 8) a second conversion unit

(item 9) and a switch (item 13) for selecting a conversion unit. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a first and second conversion unit and a switch in the second switching device of Chow in view of Matsunami and Whiting in order to properly format data received from a network (Whiting, col. 3, line 65 through col. 4, line 6; col. 4, lines 14-19).

Claims 25-26 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. (US 6,148,349) in view of Hipp et al. (US 6,325,636).

Regarding claims 25-26 and 29, Chow discloses a system (fig. 2) comprising several serverlets (items 212 and 214) each comprising a processor and memory (fig. 3, item 304) and a power conversion unit (item 306). The serverlets are coupled to a shared disk system (fig. 2, item 218 and 222) and a switch fabric network (106).

However, Chow does not disclose that the serverlets include a DIMM and that the system includes a chassis comprising first and second switching devices. Hipp discloses a system (fig. 1, item 38) comprising serverlets (item 32; fig. 2) comprising a DIMM (fig. 2, item 93; col. 10, lines 37-43), and a chassis (item 38) to house multiple serverlets. The chassis is coupled to a shared disk system (fig. 1, item 54) and includes a first switching device (fig. 1, item 48; fig. 5; col. 12, lines 37-55) to couple the severlets to the shared disk system via a bus (item 52; col. 5, lines 2-5) connecting the first switching device and the shared disk system. The system further includes a second switching device (fig. 1, item 40; col. 12, lines 37-40 and 47-50) to couple to a switched fabric network (item 45). The system also includes data buses (fig. 1, item 34) to connect the serverlets to the switching devices, where the first and second data buses are the same. The serverlets of the system (fig 10, item 32) do not include a cooling system (fig. 10, item 264-269). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to

have a server chassis for serverlets of the invention of Chow in order to simplify or make easier the implementation of several computing resources (Hipp, col. 1, line 45 through col. 2, line 21).

Regarding claim 30, Chow in view of Hipp discloses serverlets that include an internal disk system (fig. 2, item 86). In removing a disk system, the scope of the serverlet is merely broadened by eliminating elements and their functions. It has been held that omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. In re Karlson, 136 USPQ 184 (CCPA). Also note Ex parte Rainu, 168 USPQ 365 (Bd. App. 1969) (omission of a reference element whose function is not needed would be obvious to one skilled in the art). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to not have an internal disk system in the invention of Chow in view of Hipp.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow in view of Hipp as applied to claim 26 above, and further in view of Aguilar et al. (US 6,199,137).

Chow in view of Hipp discloses a data bus connecting switching devices. However, Chow in view of Hipp does not disclose the data bus is Hublink. Aguilar discloses a system bus that is Hublink, among several other standardized buses (col. 5, lines 46-48). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a Hublink bus in the invention of Chow in view of Hipp in order to provide suitable standardized interconnectivity between computer components as is known in the art.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow in view of Hipp as applied to claim 26 above, and further in view of Bealkowski et al. (US 5,465,357).

Chow in view of Hipp does not disclose accessing boot information from a disk system. Bealkowski discloses accessing boot information from a disk system (fig. 1B, col. 11, lines 29-32). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to

perform network booting for serverlets in the invention of Chow in view of Hipp in order to reduce the complexity of the serverlets (Bealkowski, col. 7, line 61 through col. 8, line 3; note: computer without a disk drive; col. 4, lines 44-46).

(10) Response to Argument

Applicant argued against the rejection of claims 1-10 and 31 over Chow in view of Matsunami. However, Examiner believes the rejection of claims 1-10 and 31 are proper for reasons indicated below.

Examiner disagrees with Applicants argument that Chow does not disclose either the recited switch coupling serverlets to a switch fabric or the recited module.

Applicant argued that if the interface 802 of Chow was a switch as described in the rejection then the function of the system of Chow would be more simplified. This simplified local routing is not mentioned in Chow, though it is not necessarily precluded. Generally, Chow mentions that BYNET networks have scalability at col. 25, lines 3-12, and have beneficial traffic shaping at col. 25, lines 26-39. The structure of BYNET appears to satisfy several criteria, especially communicating data across a network at col. 3, lines 28-35. Chow does not specifically address transmitting data between compute nodes and IONs that are within the same locality. Therefore, Examiner believes applicant's statements about simplified local routing do not have support in Chow to invalidate Examiner's ground of rejection.

Chow repeatedly mentions the connection from the IONs to the interconnect fabric as a singular entity. A "system interconnect" 228 connects at least two IONs (serverlets) to the

interconnect fabrics at col. 4, lines 46-47 and fig. 3. A "processor" 804 provides circuit control for the IONs at col. 25, lines 40-44 and fig. 8. Most importantly, a "send-side interface" controls the transmission of data for the IONs and a "receive-side interface" controls the reception of data to the memory of the IONs at col. 25, lines 44-50. Therefore, one skilled in the art would recognize that the receive-side and host-side interfaces direct data to or from at least two IONs (serverlets) and the interconnect fabrics, thereby meeting the limitation of the second switching device as recited in claim 1. Examiner considers a second switching device as a device that directs data to or from at least two serverlets, as shown in fig. 6 and described on page 9, line 20 through page 10, line 10 of the instant application.

Applicant argued that each box in Chow is a separate entity and thus the receive-side interface and the send side interface each comprises several interfaces. However, the nature the boxes is not disclosed in Chow and may not represent any logical or physical partitioning. Chow only mentions one interface having one processor for creating, controlling and removing channels at col. 25, lines 40-50.

Applicant argued that Chow does not describe a module having the two serverlets and the second switching device. Although Applicant notes that many ION cliques, compute nodes and the interface may not be in one module, the teachings of Chow in figs. 2-3 and 8 suggest having the system interconnect and receive-side or send-side interface (first switching device) coupled to two IONs (serverlets) to meet the limitations of claim 1. Examiner has considered the receive-side interface as part of the claimed system module. In figs. 2 and 3 of Chow, the system interconnect is shown coupled to the IONs and in fig. 8, the receive-side interface is shown coupled to the IONs. Therefore, Chow describes a second switch device that is part of a system module. A system module, as interpreted by the Examiner in light of the description of the instant application, is an

article that includes several components in a single assembly as described in the specification at page 9, lines 9-15. Further, Chow teaches the use of an enclosure having several components in fig. 4.

Examiner disagrees with Applicant's arguments that it would not have been obvious to modify Chow in view of Matsunami in the manner proposed by the Examiner.

Applicant recites a first switching device to couple the serverlets and the I/O resources. Examiner used the Matsunami reference to show it would have been obvious to one skilled in the art to use the first switching device instead of the connections as shown in Chow as item 216 of figs. 2 and 5. Matsunami shows a switch connecting I/O resources (diskarray subsets of fig. 1). The motivation for the combination is to enhance scalability or improve reliability as noted in Matsunami, col. 12, lines 4-14 and 25-40.

Applicant argued that the teaching of Matsunami for a switch to connect I/O resources would not benefit the system of Chow. Specifically, Applicant argued that interposing the diskarray switch between the I/O nodes and the JBODs ignores the function of the diskarray in Matsunami, further delay would be added to the BYNET of Chow using the proposed combination, and that the crossbar nature of the switch of Matsunami would undermine the function of the system of Chow by causing unavailability. However, in response to applicant's argument, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871

(CCPA 1981). It is reasonable from the disclosure of Matsunami that a switch for coupling the I/O resources (or JBODs) of Chow to the I/O nodes would have been apparent to one skilled in the art.

Examiner would like to further address Applicant's arguments that the Matsunami reference teaches away from Chow due to a bottleneck in JBOD access. In Chow each ION device must have access to the JBODs (col. 8, lines 63-67), while Matsunami similarly allows for each host device to access all disk arrays (figs. 4 and 15; col. 12, line 66 through col. 13, line 1). Although two devices must transmit through the switch, it does not appear that the packet switch of Matsunami provides excessive delay to transmitted data (figs. 5 and 7; col. 5, lines 45-55; col. 9, lines 12-24) to provide a bottleneck in the JBOD system of Chow. In Chow, there must be some delay in communication between the ION and the JBOD because of the physical nature of the system. However, Chow does not appear to disclose a limit to the delay before the system becomes inoperable. The switch of Matsunami allows any host to address to any disk as desired (col. 9, lines 12-24) and thus provides unrestricted access through the switch, as similar to the operation of the system of Chow. Therefore, it does not appear that the teaching of Matsunami would cause the system of Chow to be inoperative.

Applicant argued similarly against the rejection of claims 11-19 over Chow in view of Matsunami. However, Examiner believes the rejection of claims 11-19 are proper for reasons indicated above.

Applicant argued similarly against the rejection of claims 20-24 over Chow in view of Matsunami. However, Examiner believes the rejection of claims 20-24 are proper for reasons indicated above.

Applicant argued against the rejection of claims 25-30 over Chow in view of Hipp and Johnson. However, the Johnson reference is no longer used to reject these claims (MPEP 1207.03 (III)). The rationale stated by the Examiner in the rejection above is that the Hipp reference discloses a first switch (item 48; fig. 5) that couples the serverlets to the shared disk system, where the first switch is connected to the disk system by a bus (item 52).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

4/9/07

Kevin C. Harper

Conferees:

Lynn Field

Seema S. Rao 4/16/07

Seema Rao